
EMBER[®] EM35x NCP Host (STM32) MODULE TECHNICAL SPECIFICATION

When combined with an Ember EM35x NCP Breakout Board, the Ember STM32 NCP Host Module offers a complete ZigBee wireless solution for development and deployment of a low-data-rate, low-power ZigBee application. The STM32 microprocessor is part of the two-layer (FR4-based) host module that connects to the EM35x NCP Breakout Board through the board-to-board connectors.

This document provides the technical specification for the STM32 EM35x NCP Host Module. It describes the board-level interfaces as well as the key performance parameters. In addition, it provides the necessary information for developer to validate their application designs using the STM32 EM35x NCP Host Module.

New in This Revision

Document renumbering.

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1 STM32 Host Module Features

The STM32 EM35x NCP Host Module offers:

- ARM® Cortex™-M3 based microprocessor (STM32F103RET6)
512 kB FLASH, 64 kB RAM
- Host UART1 for use with STM32 serial bootloader and application serial UART
- Host UART2 for EZSP UART interface to EM35x NCP
- Host SPI1 for EZSP SPI interface to EM35x NCP
- 16 additional Host GPIO routed to mating connector for application use on EM35x NCP Breakout Board
- All unused Host GPIO routed to test points
- 14-pin, 0.1" pitch, dual-row, JTAG programming and debug header (could be used with a JTAG programmer such as SEGGER's JLINK.)
- 16-pin, 0.1" pitch, single-row along with a 20-pin 0.1" pitch, single-row, board-to-board connector for mating to the EM35x NCP Breakout Board
- Spare Host IO routed to test points for application use

Table 1 lists the DC electrical characteristics of the STM32 EM35x NCP Host Module.

Table 1. DC Electrical Characteristics

Parameter	Min.	Typ.	Max.	Unit
VDD supply	2.0		3.6	V
Current Draw (active)		45		mA
Operating temperature	0		+ 55	C

For more information on the STM32F103RET6, refer to the STM32 data sheet (download from <http://www.st.com/internet/mcu/product/164485.jsp>).

2 Components

Figure 1 illustrates the components on layer 1 (top side), while Figure 2 illustrates the components on layer 2 (bottom side).

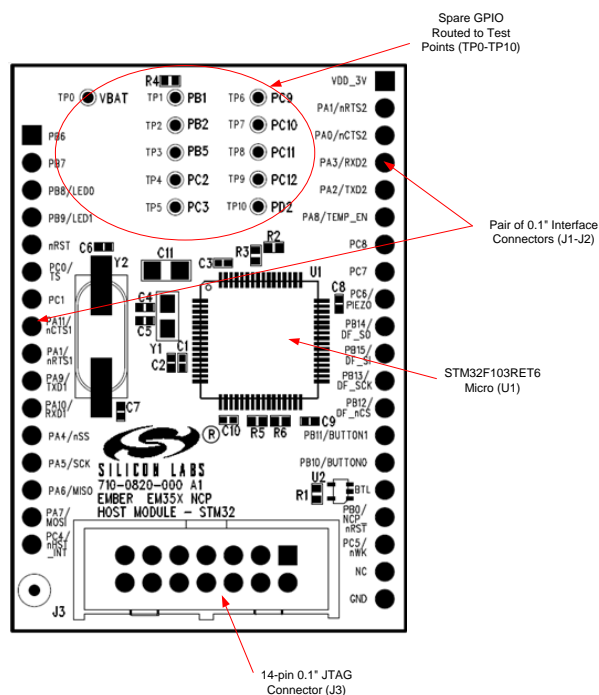


Figure 1. Assembly Print for Layer 1

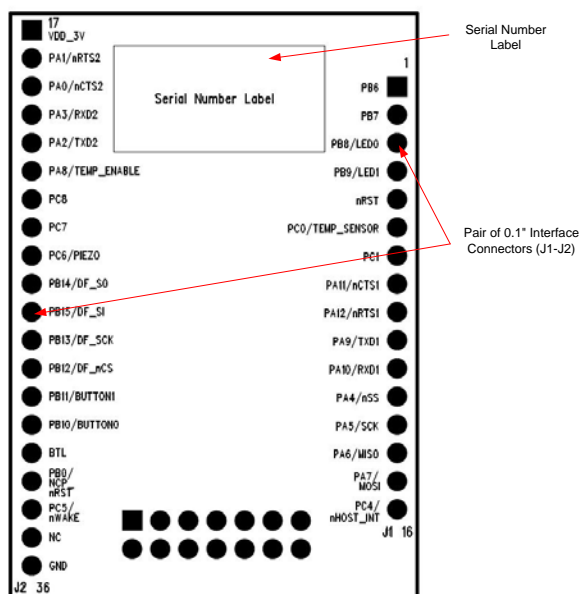


Figure 2. Assembly Print for Layer 2

2.1 STM32 Microcontroller

The STM32 NCP Host Module contains the STM32F103RET6 microcontroller from ST Microelectronics. This microcontroller is based on the Cortex-M3 core from ARM. This version of the STM32 contains 512 kB of FLASH and 64 kB of SRAM. Two USARTs are exposed to the board-to-board connector for STM32 system bootloading (STM32 USART1) and EZSP UART (STM32 USART2) to the EM35x NCP. Two SPI ports are also routed to the board-to-board connector for EZSP SPI interface to the EM35x NCP (STM32 SPI1) and external DataFlash (STM32 SPI2). Various other IOs are exposed to the board-to-board connector, including timers and interrupts. For more information on the STM32F103RET6, refer to the STM32 datasheet (download from <http://www.st.com/internet/mcu/product/164485.jsp>).

2.2 EM35x NCP Breakout Board interface connector (J1-J2)

Two single-row, 0.1" pitch, connectors make up the STM32 NCP host module interface to the EM35x NCP Breakout Board. The board-to-board connector scheme allows access to 16 Host GPIO for application purposes, along with 2 USART ports and 1 SPI port dedicated to EZSP and debug use. These 16 Host GPIO are listed in Table 2; the connector is illustrated in Figure 3. Interface connector dimensions are shown in Figure 4.

Table 2. Host GPIO Functions

Host GPIO	STM32 I/O	Primary GPIO Function
HGPIO0	PB8	Application LED (LED0)
HGPIO1	PB9	Application LED (LED1)
HGPIO2	PB10	Application Button (BUTTON0)
HGPIO3	PB11	Application Button (BUTTON1)
HGPIO4	PC6	Application Speaker (PIEZO)
HGPIO5	PC7	Spare GPIO
HGPIO6	PC8	Spare GPIO
HGPIO7	PA8	Temperature Sensor Enable (TEMP_ENABLE)
HGPIO8	PC0	Temperature Sensor ADC (TEMP_SENSOR)
HGPIO9	PC1	Spare GPIO
HGPIO10	PB6	Spare GPIO
HGPIO11	PB7	DataFlash Shutdown (DF_nSD)
HGPIO12	PB12	DataFlash SPI Chip Select (DF_nCS)
HGPIO13	PB13	DataFlash SPI Clock (DF_SCK)
HGPIO14	PB15	DataFlash SPI Serial In (DF_SI)
HGPIO15	PB14	DataFlash SPI Serial Out (DF_SO)

J1		J2	
1	PB6	VDD_3V	17
2	PB7	EZSP_nRTS2	18
3	LED0	EZSP_nCTS2	19
4	LED1	EZSP_RXD2	20
5	nRESET	EZSP_TXD2	21
6	TEMP_SENSOR	TEMP_ENABLE	22
7	PC1	PC8	23
8	SER_nCTS1	PC7	24
9	SER_nRTS1	PIEZO	25
10	SER_TXD1	DF_SO	26
11	SER_RXD1	DF_SI	27
12	nSS	DF_SCK	28
13	SCK	DF_nCS	29
14	MISO	BUTTON1	30
15	MOSI	BUTTON0	31
16	nHOST_INT	BTL	32
		NCP_nRESET	33
		nWAKE	34
		N/C	35
		GND	36

Figure 3. Board-to-Board Connector for the STM32 NCP Host Module

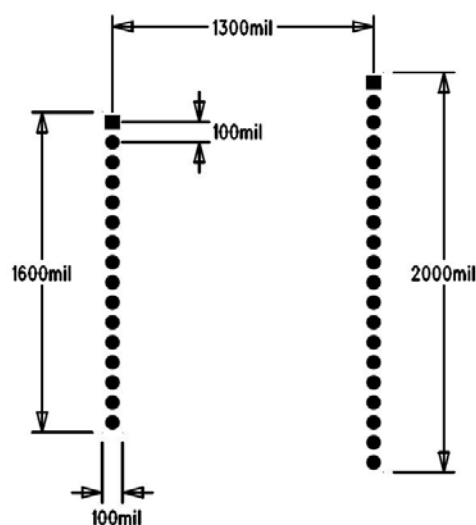


Figure 4. Board-to-Board Connector Dimensions for the STM32 NCP Host Module

Table 3 describes the pinout and signal names at J1 and J2.

For more information on the functions of the STM32 GPIO, refer to the STM32 datasheet (download from <http://www.st.com/internet/mcu/product/164485.jsp>).

Table 3. Pinout and signal names of the interface connectors

Pin #	Signal name	Direction ²	Connector	Description
1	PB6	I/O	J1	Spare STM32 GPIO (HGPI010)
2	PB7	I/O	J1	Spare STM32 GPIO (HGPI011)
3	LED0	I/O	J1	STM32 PB8 (HGPI00)
4	LED1	I/O	J1	STM32 PB9 (HGPI01)
5	nRESET	I/O	J1	STM32 Reset
6	TEMP_SENSOR	I/O	J1	STM32 PC0 (HGPI08)
7	PC1	I/O	J1	Spare STM32 GPIO (HGPI09)
8	SER_nCTS1	I/O	J1	STM32 PA11
9	SER_nRTS1	I/O	J1	STM32 PA12
10	SER_TXD1	I/O	J1	STM32 PA9
11	SER_RXD1	I/O	J1	STM32 PA10
12	nSS	I/O	J1	STM32 PA4
13	SCK	I/O	J1	STM32 PA5
14	MISO	I/O	J1	STM32 PA6
15	MOSI	I/O	J1	STM32 PA7
16	nHOST_INT	I/O	J1	STM32 PC4
17	VDD_3V	Power	J2	3V Source Pin
18	EZSP_nRTS2	I/O	J2	STM32 PA1
19	EZSP_nCTS2	I/O	J2	STM32 PA0-WKUP
20	EZSP_RXD2	I/O	J2	STM32 PA3
21	EZSP_TXD2	I/O	J2	STM32 PA2
22	TEMP_ENABLE	I/O	J2	STM32 PA8 (HGPI07)
23	PC8	I/O	J2	Spare STM32 GPIO (HGPI06)
24	PC7	I/O	J2	Spare STM32 GPIO (HGPI05)
25	PIEZO	I/O	J2	STM32 PC6 (HGPI04)
26	DF_SO	I/O	J2	STM32 PB14 (HGPI015)
27	DF_SI	I/O	J2	STM32 PB15 (HGPI014)
28	DF_SCK	I/O	J2	STM32 PB13 (HGPI013)
29	DF_nCS	I/O	J2	STM32 PB12 (HGPI012)
30	BUTTON1	I/O	J2	STM32 PB11 (HGPI03)
31	BUTTON0	I/O	J2	STM32 PB10 (HGPI02)
32	BTL	I	J2	Inverted and routed to STM32 BOOT0
33	NCP_nRESET	I/O	J2	STM32 PB0
34	nWAKE	I/O	J2	STM32PC5
35	NC	N/A	J2	Not connected
36	GND	Power	J2	Ground connection

² with respect to the STM32

2.3 JTAG Programming and Debug Connector (J3)

The STM32 NCP Host module includes a 14-pin 0.1" dual-row header for JTAG programming and debug access. Figure 5 shows the pinout of this header. Note that the EM35x NCP Kit does not ship with a programmer that interfaces to this header. Third-party programmers may connect to this header. For example, the J-Link ARM 14-

pin Adapter from SEGGER (<http://www.segger.com/cms/jlink-adapters.html#14pinAdapter>) may be connected directly to this header.

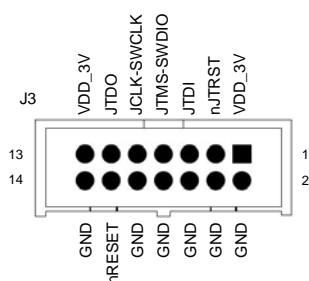


Figure 5. JTAG Connector Pinout (J3)

2.4 Unused STM32 GPIO (TP0-TP10)

The STM32 NCP Host module routes all GPIO not routed to the mating connectors to test points TP0 through TP10. This allows the developer to utilize all STM32 GPIO for their application, if required. Table 4 lists these test points.

Table 4. STM32 Unused GPIO Routed to Test Points


Test Point	Signal name	Test Point	Signal name
TP0	VBAT	TP6	PC9
TP1	PB1	TP7	PC10
TP2	PB2_BOOT1	TP8	PC11
TP3	PB5	TP9	PC12
TP4	PC2	TP10	PD2
TP5	PC3		

3 STM32 NCP Host Module Schematic

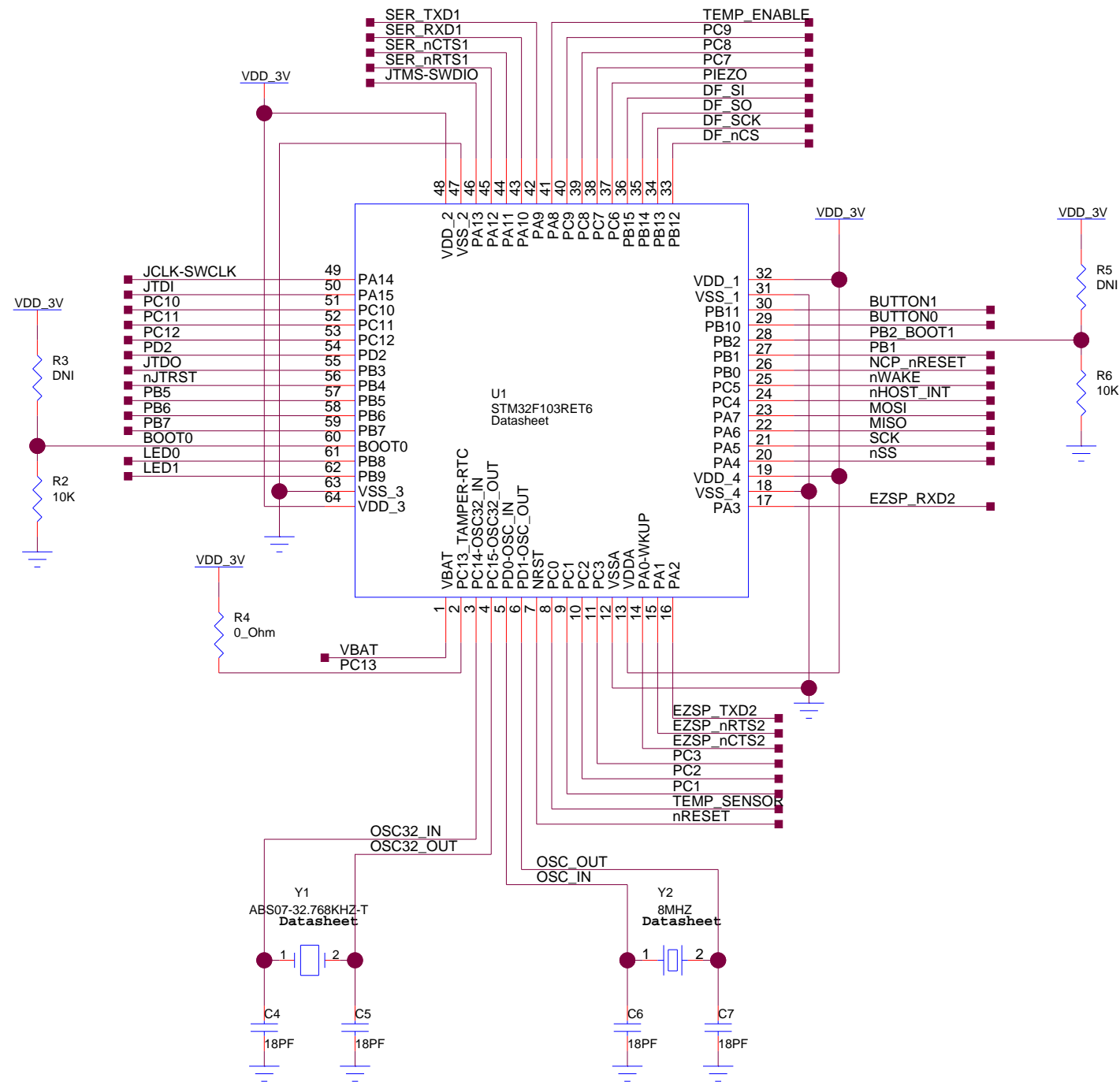
The STM32 NCP Host Module schematic is included at the end of this document.

EM35x NCP Host Module (STM32)

Sheet	Details
1	COVER SHEET
2	STM32 MICRO, INTERFACE CONNECTORS
3	REVISION NOTES

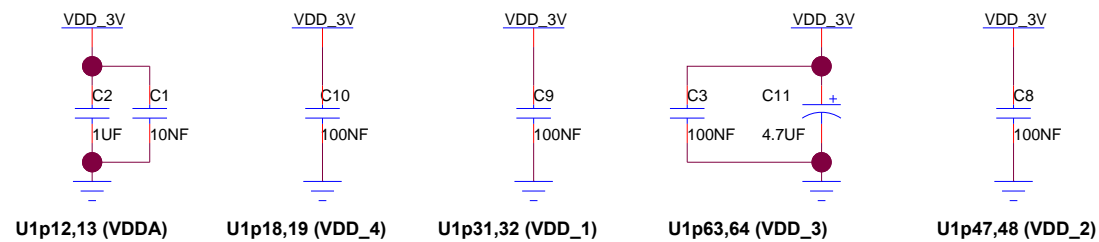
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DWG	SCH0820		REV A0
TITLE	EM35X NCP HOST MODULE (STM32)		
PAGE	COVER SHEET		
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STM32 EZSP Host Micro

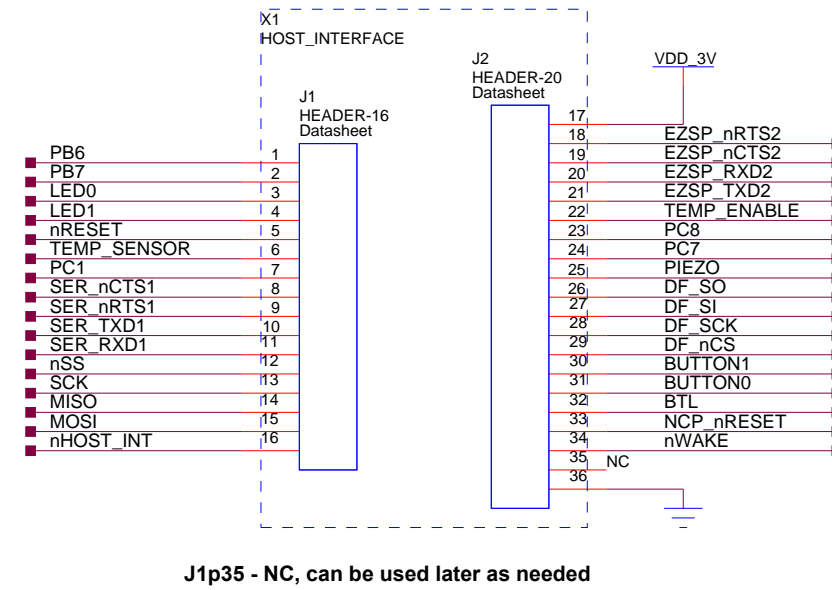


Power Supply Decoupling

NOTE: Place as close to noted U1 pins as possible

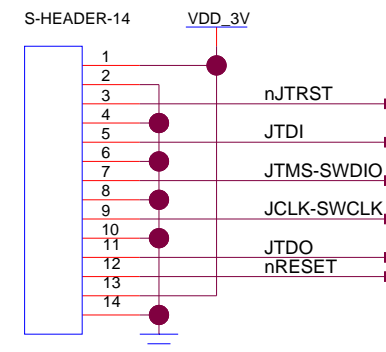


EM35x EZSP Breakout Board Interface Connectors

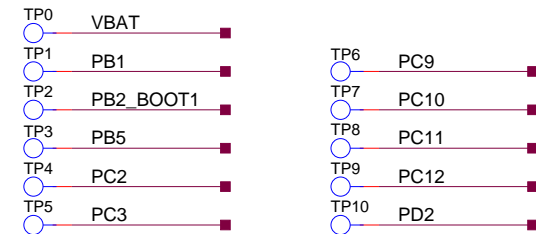


JTAG Connector

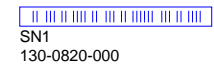
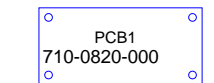
Datasheet
J3



Test Points - Unused IO



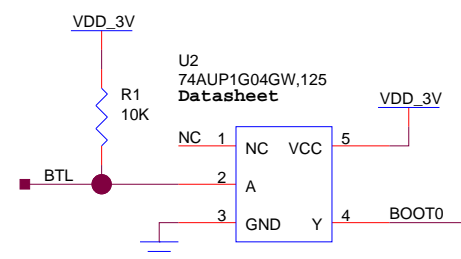
PCB Information




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Bootload Signal Inverter



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SCHEMATIC NOTES:

-- Version P0 --
*Released: 2010-06-11
*Initial version released, Version P0 (initial draft)

-- Version P1 --
*Released: 2010-08-03
*Changes from P0 to P1:
1) Swapped UART1 with UART2 on X1 (J1, J2).
2) Changed R2 from 0 ohm to 10k ohm.
3) Changed R6 from DNI to 10k ohm.
4) Changed U1.27 net connection from BTL to PB1.
5) Change TP1 to TP0 for VBAT net.
6) Added TP1 for PB1 net.
7) Added inverter IC U2 for inverting BTL net for connection to BOOT0 net.


-- Version A0 --
*Released: 2010-09-20
*Production version release
*Changes from P1 to A0:
1) Removed DS1 and R1 for lowest current capability.
2) Renamed UART1 nets to SER_TXD1, etc.
3) Renamed UART2 nets to EZSP_TXD1, etc.
4) Added 10k pull-up R7 to U2 BTL net.
5) Updated title from EZSP to NCP.
6) Corrected DF_SO/_SI error at X1 J2p26/27 (reversed).
7) Removed Packet Trace Port connector footprint J4.
8) Replaced J3 with 14-pin 0.1" JTAG connector.

PCB LAYOUT NOTES:

-- Version P0 --
*Released: 2010-06-11
*Initial version released, Version P0 (initial draft)

-- Version P1 --
*Released: 2010-08-03
*Changes from P0 to P1:
1) Added Inverter IC U2.
2) Re-routed UART1 and UART2 nets.
3) Added missing test points from P0 version.

-- Version A0 --
*Released: 2010-09-20
*Changes from P1 to A0:
*Production version release
1) All schematic notes reflected in layout.

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